Study of body factor and inversion charge density dependence on temperature in UTBB SOI MOSFETs

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***Abstract*—The aim of this work is to study the behavior of body factor and inversion charge density of UTBB SOI MOSFETs with different channel lengths from room temperature up to 425 K. Such parameters are important to investigate the electrostatic integrity of devices. The analysis is based on physical device simulation and previously published models. The results showed that body factor and inversion charge density has a percentage increase around of 4.2 % with temperature and 7.7 % with L, due to the influence of source and drain regions and Short Channel Effects (SCE).**

Keywords—body factor, inversion charge density, temperature, UTBB SOI MOSFETs, numerical simulations.

I. INTRODUCTION

The Ultra-Thin Body and Buried Oxide (UTBB) SOI MOSFET has been considered for future technologic nodes, due to its improved electrostatic control, high immunity to local doping variation and multiple threshold voltages achieved by different back-gate bias [1, 2]. Namely, the reduction of both the silicon film thickness (t_{Si}) and buried oxide thickness (t_{BOX}), can help significantly the device downscaling. Without BOX scaling, a 3 nm SOI film is required for the 8nm node, while it can be kept around 5 nm, if the BOX is scaled down below 10 nm [1]. Usually, UTBB devices have t_{BOX} dimensions between 10 and 30 nm and t_{Si} around 7-10 nm [3].

The temperature effects in UTBB SOI MOSFETs are important even for room-temperature applications, as these devices can be affected by self-heating with channel temperature reaching ~ 400 K under normal operation conditions [4, 5].

The focus of this work is to analyze the body factor (n) and inversion charge density (Q_{TH}) behavior with temperature (T), in order to study the electrostatic control of UTBB devices for different channel lengths at higher temperatures. In [6], an experimental analysis of DIBL as a function of temperature was made and a model for DIBL(T) was proposed. Such model depends on the extraction of inversion charge density. However, the behavior of Q_{TH} and its physical aspects were not investigated yet, besides its relation with the body factor [7]. In [8] the body factor of UTBB is analyzed according the supercoupling effect. In [9] the behavior of Q_{TH} is studied according to the strong inversion threshold and intrinsic threshold. In [10] the inversion charge is analyzed considering quantum effects in Tri-Gate MOSFETs. Hence, a study of n and Q_{TH} in UTBBs as a function of temperature were not performed until now.

In this work, the simulated values are compared with analytical models and the temperature dependence was included in the models by using the vertical channel position, which was extracted from simulated structures for each temperature.

II. NUMERICAL SIMULATIONS

A. Device characteristics

A cross-section of the UTBB MOSFET structure is illustrated in Fig. 1, where t_{ox} is the gate oxide thickness, t_{Si} is the silicon film thickness and t_{BOX} is the buried oxide thickness, V_{GS} is the gate voltage and V_{GB} is the back-gate voltage.

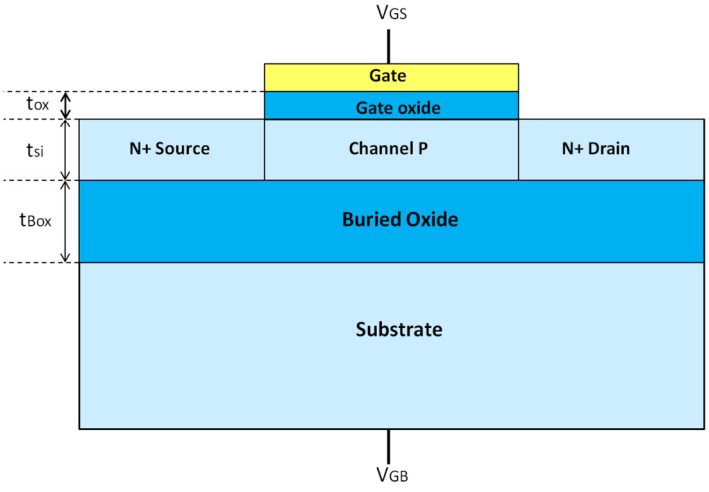

Fig. 1 Cross-section of UTBB Transistor.

Two-dimensional numerical simulations were performed using Silvaco ATLAS device simulator [11]. The simulated devices have the characteristics of 28nm node of ST Microelectronics [12] as follows: channel lengths from 40 nm up to 500 nm, t_{si}=7 nm, t_{ox}=1.3 nm, t_{BOX}=25 nm, channel doping concentration (N_A) of $1x10^{15}$ cm^{-3} and source and drain doping concentration (N_D) of $1x10^{20}$ cm^{-3}. For each channel length, simulations with temperatures of 300, 325, 350, 375, 400 and 425 K were performed, including the physical models of Klassen and Shirahata for mobility, SRH (Shockley-Read-Hall) for recombination of carriers, BGN for bandgap narrowing. All physical models were used with the default parameters as implemented in Atlas device simulator [11].

B. Electrical characteristics

The simulations were performed for a low drain bias (V_{DS}=50 mV), V_{GB}= 0 and V_{GS} varying from 0 up to 1 V. Besides, the structure files were saved at threshold condition in order to analyze the electron concentration and extract the channel position in the silicon film.

Fig. 2 shows the $I_{DS}xV_{GS}$ curves for different channel lengths at room temperature. As the curves are being presented in a subthreshold regime, it is known that in this condition, the curves are degraded according to the reduction of the channel length.

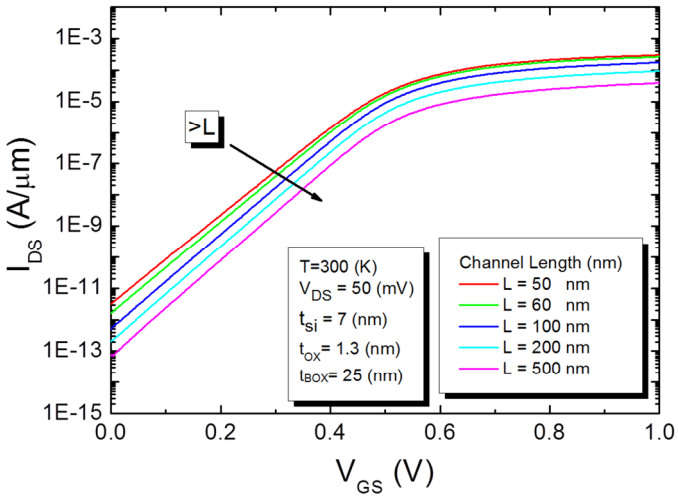

Fig. 2 Drain current as a function of gate voltage at room temperature.

III. Results and Discussion

Fig. 3 shows the threshold voltage (V_{TH}) as a function of temperature. The V_{TH} values were extracted using the transconductance derivative method [13]. It is worth noting that V_{TH} increases with the rise of channel length, because the temperature accentuates the Short Channel Effects (SCE) [14]. When the increase of temperature occurs, the intrinsic carrier concentration increases and the Fermi potential (Φ_F) is reduced, causing the V_{TH} reduction.

Fig. 4 shows the subthreshold swing (S) as a function of temperature. S values were extracted from simulations results using the maximum of gm/I_{DS} ratio, that is, the subthreshold region [15], where gm is the transconductance. S is proportional to thermal potential (k*T/q), hence, to temperature [14]. Notice that the S degradation with L reduction became more significantly as the temperature increases, the same behavior observed in Fig. 3.

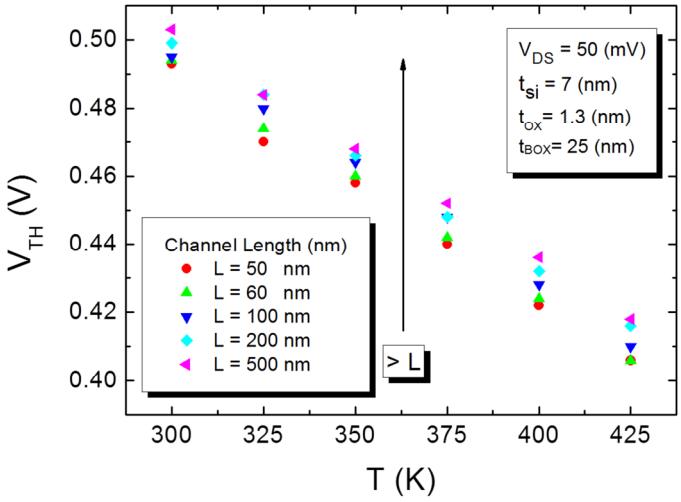

Fig. 3 Threshold voltage as a function of temperature for different channel lengths.

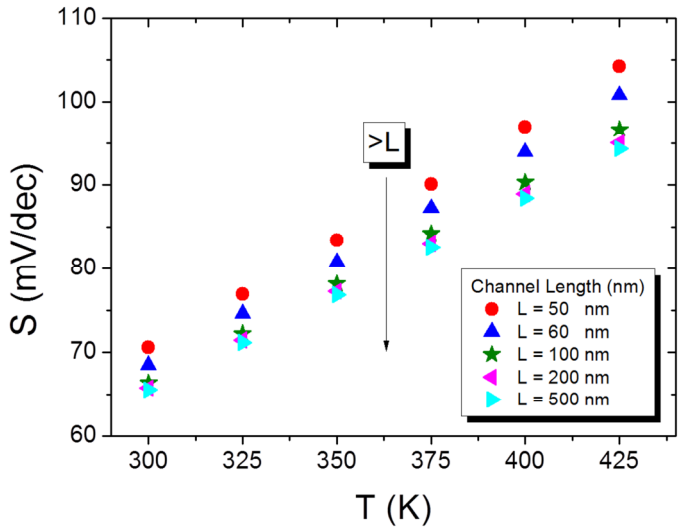

Fig. 4 Subthreshold slope as a function of temperature for different channel lengths.

The body factor (n) was extracted from simulations, using the same method of S extraction. The relation between the n and S is showed in (Eq. 1):

$$n = \frac{S}{\left(\frac{k.T}{q}\right)ln(10)} \quad (1)$$

The *n* values were also compared to analytical model. In order to adapt the model for different temperatures, the vertical channel position in the silicon film (Y_{MEAN}) was extracted from the electron concentration in the center of channel as indicated in [16] and presented in (Eq. 2):

$$Y_{MEAN} = \frac{\int_0^{tsi}(y.eC)dy}{\int_0^{tsi}(eC)dy} \quad (2)$$

where y is the vertical position along t_{si} and eC is the electron concentration at threshold condition. Fig. 5 shows the vertical cut that was made in the center of the channel to extract the electron concentration and consequently, Y_{MEAN}.

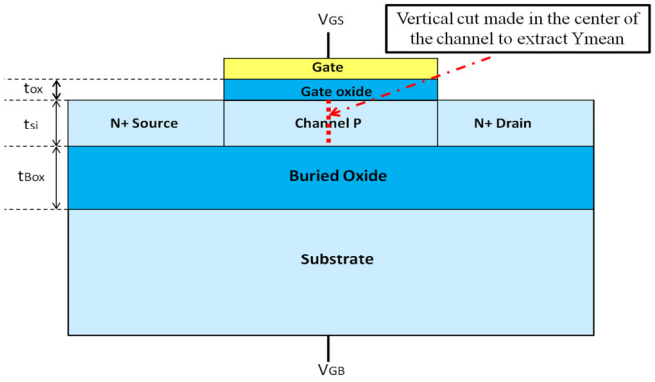

Fig. 5 Representation of the vertical cutline made in the center of channel to extract the Y_{MEAN} values.

Fig. 6 presents Y_{MEAN} as a function of temperature. It can be observed that the vertical position of channel moves towards t_{BOX} as the temperature increases. For the higher channel lengths Y_{MEAN} values are almost the same. As the channel length is reduced, the Y_{MEAN} values are increased, due to higher influence of source and drain carriers in the channel region.

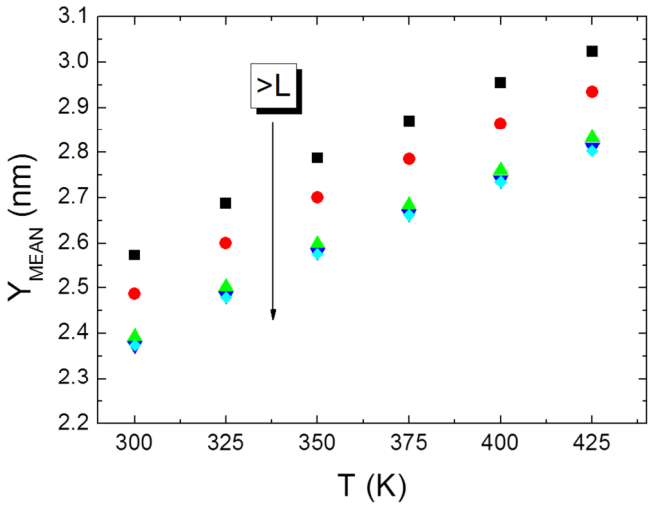

Fig. 6 Vertical position of channel as a function of temperature for different channel lengths.

The body factor (n) represents the coupling between the interfaces of the transistor. It is described by the association of capacitances between the gate and substrate terminals. For a FDSOI transistor with the second interface depleted it can be calculated according to (Eq. 3) [14]:

$$n = 1 + \left[\frac{C_{Si}.C_{BOX}}{C_{OX}.(C_{Si}+C_{BOX})}\right] \quad (3)$$

where C_{Si} is the silicon film capacitance, C_{BOX} is the buried oxide capacitance and C_{OX} is the gate oxide capacitance.

The model of (Eq. 3) was used to calculate the theoretical values of the body factor. The influence of temperature was included using the Y_{MEAN} values (Fig. 6) in the capacitances C_{Si} e C_{OX} according to (Eq. 4a and 4b) [16]:

$$C_{Si} = \frac{\varepsilon_{Si}}{(t_{Si}-Y_{MEAN})} \quad (4a)$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX} + (\frac{\varepsilon_{Si}}{\varepsilon_{OX}})Y_{MEAN}} \quad (4b)$$

Fig. 7 shows the body factor as a function of temperature. The full symbols are the extracted values from gm/I_{DS} method and it is known that values of n depend on S values as we can see according to (Eq. 1). The empty symbols are the model values. The n trends are the same of subthreshold slope observed in Fig. 4. Notice that the model values do not reproduce the extracted ones, which indicates that Y_{MEAN} is not enough to represent the body factor dependence on temperature. Regarding the channel length, a percentage variation of 7.7 % was obtained at room temperature.

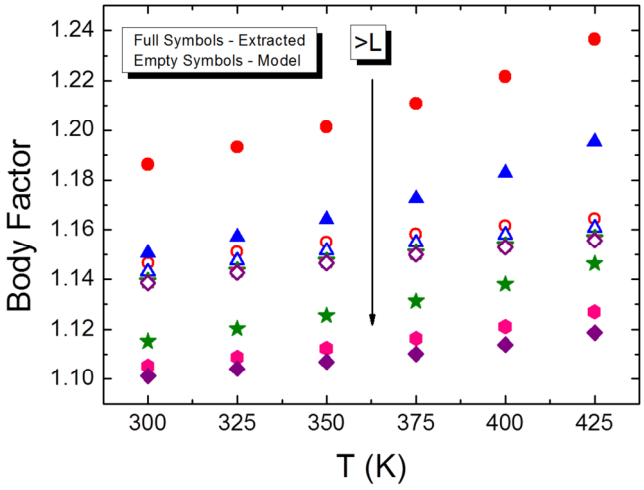

Fig. 7 Body factor as a function of temperature for different channel lengths.

Such behavior is evidenced in Fig. 8, which presents the body factor variation with temperature (Δn/ΔT) as a function of channel length. It can be noticed that the variation of the extracted values much higher than the model ones, especially in short channel devices.

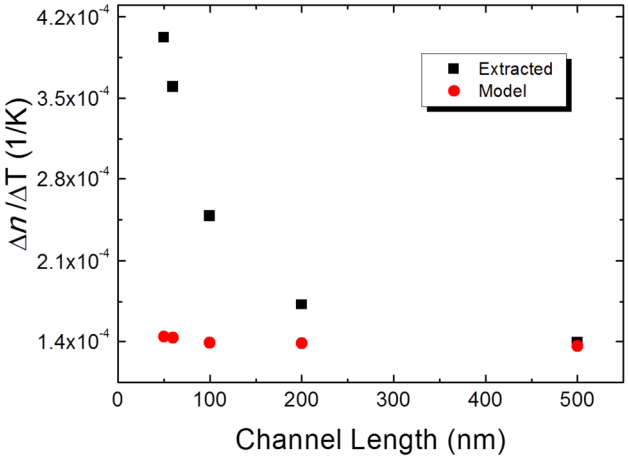

Fig. 8 Body factor variation with temperature as a function of channel length.

The body factor can be used to predict the inversion charge density (Q_{TH}). This relation is presented in (Eq. 5) [14]:

$$Q_{TH} = n.\left[\frac{\left(\frac{k*T}{q}\right)*C_{OX}}{2*q}\right] \quad (5)$$

The extracted body factor values shown in Fig. 7, were used to calculate the Q_{TH} values presented in Fig. 9. There is an increase of 7.70 % in the inversion charge density comparing the smallest and longest channels at room temperature, due to the influence of source and drain regions.

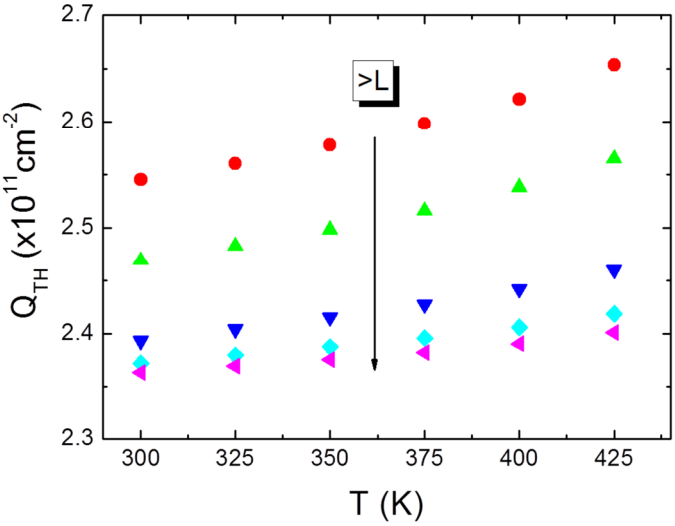

Fig. 9 Inversion charge density as a function of temperature for different channel lengths.

Table 1 presents the percentage variation of Q_{TH} with temperature for different channel lengths. The values indicate that the temperature intensify the short channel effects, thus, it is important to take the temperature into account to define the electrostatic criteria of such devices.

TABLE I. PERCENTAGE VARIATION OF Q_{TH} WITH TEMPERATURE

L (nm)	Q_{TH} variation with temperature (%)
500	1.56
200	1.94
100	2.75
60	3.93
50	4.22

IV. CONCLUSIONS

This study analyzed the body factor and inversion charge density dependence on temperature for UTBB SOI MOSFETs with channel lengths from 50 to 500 nm. The subthreshold slope remains under 102 mV/dec until the temperature of 400 K. The body factor has a percentage increase of 4.22 % with temperature and 7.72 % with L, due to the influence of source and drain regions. The body factor values were also compared to an analytical model. The temperature dependence was included in model trough the vertical channel position (Y_{MEAN}), extracted from the simulated electron concentration for each temperature. It was noticed that this parameter is not enough to reproduce the variation observed in extracted values. Regarding the inversion charge density, there is an increase of 7.70 % in the inversion charge density comparing the smallest and longest channels at room temperature. The percentage variation with temperature is about 4.22 % for the smallest L, which indicates that the temperature intensify the short channel effects, thus, it is important to take the temperature into account to define the electrostatic criteria of such devices.

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